REMARKS

Claims 1-8 and 12-30 were rejected by the Examiner in the Office Action dated July 11, 2008. Claims 12-13 and 20-30 are canceled without disclaimer and prejudice. Claims 14-19 are currently amended. New claims 31 and 32 have been added and are fully supported by the specification. No new matter has been added.

Claim Rejections Under 35 U.S.C. §103

Claims 1-8, and 13-29 are rejected under 35 U.S.C. §103(a) as being unpatentable over Intel, Inc. (IA-32® Architecture Software developer's Manual, Volumes 1-2, 2002) ("Intel"), in view of U.S. Patent No. 5,420,992 to Killian ("Killian").

Claims 12 and 30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Intel, Inc. (IA-32® Architecture Software developer's Manual, Volumes 1-2, 2002) ("Intel") in view of U.S. Patent No. 5,420,992 to Killian ("Killian") in view of U.S. Patent No. 6,219,833 to Solomon ("Solomon").

It is respectfully asserted that Intel, alone or in combination with Killian, fails to teach or render obvious the claim 1 limitation of "common subcircuitry operable to perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of said immediate field in branch instructions to calculate a target address for branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions."

While the secondary reference Killian does disclose a circuit for performing sign extension, it does not teach or disclose a circuit for performing sign extension that supports multibyte branch extensions operable to access other instructions at byte aligned addresses. This is a nonobvious and nontrivial improvement as noted in the present application in at least the last two paragraphs of the description for Figure 3, reproduced below.

> Although both the branch instruction and the add integer instruction perform sign extension operations on the immediate field value, the branch instruction multiplies the immediate field value by four before performing the sign extension. The multiplication is performed to allow for word alignment and an expanded target branch address range. However, by requiring a

multiplication of four before performing the sign extension, different subcircuitry route is required to perform the operation. In many instances, one subcircuit is specifically configured to sign extend an immediate field and another subcircuit is specifically configured to perform a sign extend of an immediate field multiplied by four. In some examples, multiplication by four is performed by using additional multiplexers and shifters on a base sign extended subcircuit. However, having additional hardware or additional subcircuits is expensive, particularly for programmable chips. Consequently, and the techniques and mechanisms of the present invention allow the reuse of subcircuitry for both types of instructions.

Techniques and mechanisms of the present invention allow the units of branch instructions to be in bytes even though many of the instructions are multiple bytes in size and a required to be aligned on multi-byte addresses.

Therefore, Killian does not rectify the lack in teachings of Intel, and it is submitted that the combination of Intel and Killian fails to render independent claim 1 and all the claims that depend therefrom obvious.

Claim 14 has been amended to recite "A field programmable gate array, comprising circuitry configured to process a plurality of branch and non-branch instructions associated with an instruction set, the plurality of branch instructions and non-branch instructions including an immediate field; and common subcircuitry that performs a sign extension of an immediate field associated with one or more branch instructions and that performs a sign extension of said immediate field associated with one or more non-branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions, wherein the sign extension of the immediate field associated with one or more branch instructions is performed to determine a branch target address."

Intel, alone or in combination with Killian and Solomon, fails to teach such a field programmable gate array ("FPGA"). Additionally, one of skill in the art would not consider such an FPGA obvious, as there is nothing within the cited references that would lead to the features and functionality of the claimed FPGA. Those of skill in the art also understand that the architecture and techniques utilized in a conventional general purpose processor are not necessarily implemented or in some situations feasible in an FPGA.

While Solomon discusses use of a secondary processor 4, such as an FPGA, as a dedicated coprocessor adapted to handle a specific function, this is in no way related to the claims of the present application. See Solomon Col. 4, lines 43-66. In Solomon, "each secondary processor 2, 4 is adapted to increase the computational power and efficiency or the architecture by handling parts of the source code not well handled by the primary processor 1." Solomon at Col. 4, lines 50-53. Again, this is not relevant to the claims of the present application. Furthermore, Solomon makes it clear that "such coprocessors 4 are not the specific subject of the present application." Solomon at Col. 4, lines 58-59.

Therefore, it is respectfully asserted that independent claims 1, and 14 and all the claims that depend therefrom are in condition for allowance. With regard to dependent claim 18, it is submitted that Intel, alone or in combination with Killian and Solomon fails to teach the amended limitation "wherein common subcircuitry is used to handle the immediate field associated with the branch and non-branch instructions and wherein an immediate field value is maintained in units of bytes."

New claims 31 and 32, reproduced below, are also not taught by Intel, alone or in combination with Killian and Solomon.

> 31.   (New) The processor of claim 1, wherein one of a primary or secondary component accesses memory of the array directly through ports without access through a system bus, and wherein the array does not comprise a system bus.

> 32.   (New) The field programmable gate array of claim 14, wherein one of a primary or secondary component accesses memory of the programmable logic device directly, without gaining access through a system bus.

Therefore it is respectfully submitted that all the pending claims are novel and non obvious.

Information Disclosure Statement

A Supplemental Information Disclosure Statement is being filed herewith. It is respectfully requested that this Supplemental Information Disclosure Statement be considered and the PTO Form 1449 be initialed and returned with the next Action.

CONCLUSION

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. Should the Examiner believe that a telephone conference would expedite the prosecution of this application; the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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